ADVANCED FUNCTIONAL MATERIALS
www.afm-journal.de

Materials Views
www.MaterialsViews.com

32 × 32 Crossbar Array Resistive Memory Composed of a Stacked Schottky Diode and Unipolar Resistive Memory

*Gun Hwan Kim, Jong Ho Lee, Youngbae Ahn, Woojin Jeon, Seul Ji Song, Jun Yeong Seok, Jung Ho Yoon, Kyung Jean Yoon, Tae Joo Park, and Cheol Seong Hwang**

Various array types of 1-diode and 1-resistor stacked crossbar array (1D1R CA) devices composed of a Schottky diode (SD) ($Pt/TiO_2/Ti/Pt$) and a resistive switching (RS) memory cell ($Pt/TiO_2/Pt$) are fabricated and their performances are investigated. The unit cell of the 1D1R CA device shows high RS resistance ratio (≈10^3 at 1.5 V) between low and high resistance state (LRS and HRS), and high rectification ratio (≈10^5) between LRS and reverse-state SD. It also shows a short RS time of <50 ns for SET (resistance transition from HRS to LRS), and ≈600 ns for RESET (resistance transition from LRS to HRS), as well as stable RS endurance and data retention characteristics. It is experimentally confirmed that the selected unit cell in HRS (logically the "off" state) is stably readable when it is surrounded by unselected LRS (logically the "on" state) cells, in an array of up to 32 × 32 cells. The SD, as a highly non-linear resistor, appropriately controls the conducting path formation during the switching and protects the memory element from the noise during retention.

1. Introduction

Resistance switching random access memory (ReRAM) has been considered as one of the most promising next-generation non-volatile memory devices as the down-scaling of charge-based memory, such as dynamic random access memory (DRAM) and flash memory, approaches physical limitations.[1–5] The primary merit of ReRAM over DRAM and flash memory lies the fact that its performance degradation with size scaling is much less severe than in charge-based memories, or becomes even better with size scaling. Another key feature of this type of memory compared with the charge-based memories is that it does not require supreme performance of the selection transistor (fully ON during writing and reading but fully OFF during data retention, which can hardly be met simultaneously in highly scaled metal-oxide-semiconductor field-effect transistors), because there is no need for the charge retention.[6,7] This allows the device architecture to change from the 1 transistor 1 capacitor (1T1C) in DRAM to 1 diode 1 resistor (1D1R) in memories based on resistance switching (RS), where the 1D1R architecture is already in use for phase change RAM.[8,9] A diode is a two-terminal device, while a transistor is a three-terminal device, making the area scaling of memory cell using diodes fundamentally beneficial compared with the case with transistors. This merit can be optimally realized with crossbar array (CA) structure, in which a memory cell composed of a stacked diode and RS element is interposed between two crossing metal lines (bit- and word-lines). One of the structures of the 1D1R CA device is schematically shown in **Figure 1**a, where the diode (upper portion) and RS memory (lower portion) are separated by a middle electrode (more details for this structure are described below). The electrically insulating nature of many oxide-based RS materials makes the fabrication of this type of structure easier since the electrical isolation between the neighboring memory cells is naturally attained, which cannot be expected from phase change materials.

The role of the diode in such CA structure is to suppress the so-called sneak current, represented by the dashed lines in Figure 1a, which disturbs the data reading and increases power consumption. Such a functionality of the circuit element can be obtained from a diode (Schottky type or p-n junction type) for the unipolar RS (URS) memory cell,[10–13] or materials with highly non-linear current–voltage (I–V) characteristics, such as threshold switches[14–17] and mixed electronic-ionic conductors[18] for the bipolar RS (BRS) cells. For any of these selection elements, the required performance specifications for high density (>1 Mb per block) are very strict due to the parallel geometry of the CA structure. The representative specifications include the very high rectification ratio (>approx. 10^6 at operation voltage) and forward current density (≈10^6 Acm^{-2}). This has been discussed in detail elsewhere.[6,19,20] The authors recently reported that such

G. H. Kim, J. H. Lee, Y. Ahn, W. Jeon, S. J. Song, J. Y. Seok, J. H. Yoon, K. J. Yoon, Prof. C. S. Hwang
WCU Hybrid Materials Program
Department of Materials Science and Engineering and Inter-university Semiconductor Research Center
Seoul National University
Seoul 151-744, Korea
E-mail: cheolsh@snu.ac.kr
Prof. T. J. Park
Department of Materials Engineering
Hanyang University
Ansan, 426-791, Korea

DOI: 10.1002/adfm.201202170

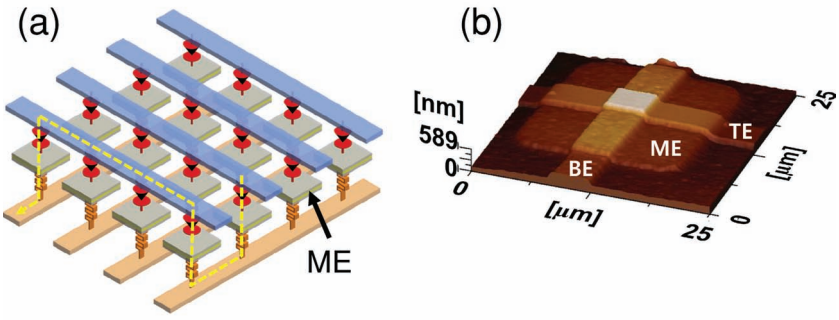

Figure 1. a) A schematic diagram of the 1D1R CA device. b) An atomic force microscopy image of the fabricated CA device with a top and bottom electrode line width of 4 μm.

functionality can be simultaneously achieved from a Schottky type diode (SD) composed of $Pt/TiO_2/Ti/Pt$ structure, while all other candidates have seldom shown such performance.[13] In the present work, therefore, CA devices with a stacked SD and URS memory cell were fabricated, and highly promising electrical performances were demonstrated. The device structure is production-friendly because of the simple material and fabrication process; both SD and URS memory ($Pt/TiO_2/Pt$) adopted atomic layer deposited (ALD) TiO_2 as the key functional material. This type of work appears to be a somewhat straightforward outcome of the research once development of the SD and URS memory are accomplished. However, it was in fact not that straightforward to attain satisfactory device performances due to various parasitic effects during the stacked device fabrication and electrical characterization. Especially, the extreme parallel geometry of the CA structure required highly uniform performance of all the memory cells in the given CA, otherwise any of the fault (or shorted) cells really disturb the measurement of any other cell or even the whole device. It appears that this constitutes the main reason why there have not been many reports on CA devices with stacked selection and memory elements with a meaningful integration density (at least >1 kb). In this work, the authors report a fully functional CA ReRAM with highly promising performance in an up to 32 × 32 memory block size. A similar work has been reported only recently by Kim et al.[21] Since the primary goal of the work is to fabricate working devices with reasonable array density and examine the memory functionality in actual device geometry, miniaturization of the cell into the nanometer range was not pursued. The minimum feature line width was limited to 2 μm, which is believed to be reasonably small to achieve the goal of this research. Further miniaturization is under way.

This report is composed of three main parts. First, key features for the fabrication processes of the CA devices are discussed. Second, the device characteristics of a single stacked cell which is fundamentally free from the influence of neighboring cells are elucidated. Finally, the memory array characteristics are explained in detail. It was indeed found that the high performance of the SD adopted in this work really suppressed the parasitic effects from the neighboring cells, and the SD works as an appropriate variable load resistor which actually improved the switching performance of the URS memory.

2. Integration of Stacked 1D1R Device Using an Oxygen Barrier Layer

The SD in this work is composed of top metal line (Word-line, WL, shown in blue in Figure 1a), which is composed of stacked 50-nm-thick Au/50-nm-thick Pt layers, a 31.5-nm-thick TiO_2 layer, a 100-nm-thick Ti, and a 30-nm-thick Pt bottom electrode. TiO_2 film was deposited by thermal ALD. The interface between the top Pt and TiO_2 forms a Schottky contact, and the TiO_2/Ti interface comprises quasi-Ohmic contact. While the top electrode of the SD has the line form (width varied from 2 to 10 μm) to make the array structure, the bottom electrode has a square shape (14 × 14 μm^2) to isolate the memory cell from neighboring cells. The URS memory cell is made of square-shaped 30-nm-thick Pt top electrode (14 × 14 μm^2), a 60-nm-thick TiO_2 layer deposited by plasma-enhanced ALD (PEALD), and line-shape stacked 50-nm-thick Pt/50-nm-thick Au layers (Bit-line, BL, shown in yellow in Figure 1a, width varied from 2 to 10 μm). Since the bottom electrode of the SD and top electrode of URS memory are commonly square-shaped 30-nm-thick Pt, the single 30-nm-thick Pt layer could be considered as the common electrode for the two circuit elements. However, as shown later, this cannot be the case due to the severe degradation of the memory performance by the fabrication of an SD on top of the single Pt layer when it was used as the middle electrode (ME, see Figure 1a). The first important step to fabricate this 1D1R CA device was, therefore, to make the appropriate ME, as discussed in detail below.

The fabrication sequence could be reversed, with the SD made first on the SiO_2/Si substrate followed by the memory subsequently being fabricated. However, this induced a severe degradation of SD performance due to the degradation in the rectifying performance of the Pt/TiO_2 interface. Figure S1a in the Supporting Information shows a typical *I–V* curve of the SD with the latter fabrication sequence revealing the improper rectifying properties.

Figure 1b shows an atomic force microscopy image of the fabricated CA device with a line width of 4 μm. TE and BE indicate the top and bottom electrodes, respectively, and the dimension of ME must be wider than the width of TE and BE in order to alleviate the direct contact between the SD and memory dielectrics without intervening ME, otherwise the device would malfunction. Figures S1b,c (Supporting Information) show the highly rectifying characteristics of the SD and unipolar switching *I–V* curve of the URS memory cell, respectively, where the SD and URS memory cells were not stacked.

Figure 2a shows the switching electrical characteristics of 1D1R CA with and a line width of 2 μm and 32 (WL) × 1 (BL) configuration, which is designed to alleviate the sneak current irrespective of the performance of the SD. In this structure, the ME was composed of 30-nm-thick Pt/30-nm-thick Au/30-nm-thick Pt, or 30-nm-thick Pt/30-nm-thick Ni/30-nm-thick Pt layers. Figure 2b shows the cross-section scanning electron microscopy (SEM) image of the stacked device, where the 30-nm-thick Ni layer was interposed between the two Pt layers

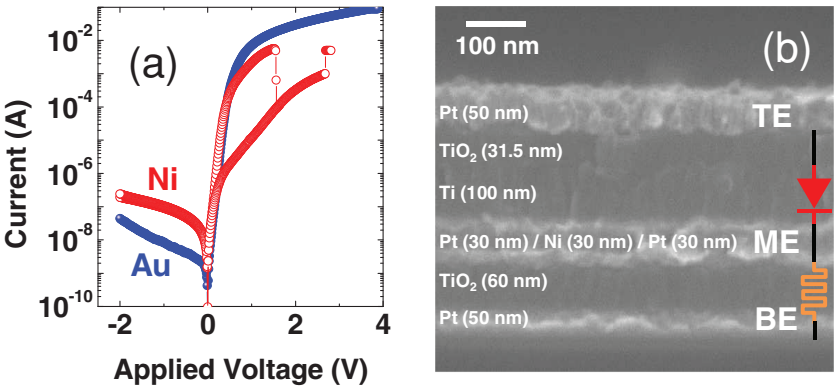

Figure 2. a) The electrical characteristics of 1D1R CA device with Ni (red symbol) and Au (blue symbol) as OBLs. b) The cross-section SEM image of 1D1R CA device with Ni as OBL.

in the ME. Here, Au or Ni layer was used as the oxygen barrier layer (OBL), which prohibits the diffusion of oxygen from the TiO_2 layer in the URS memory to the Ti layer in the SD during the fabrication process. When the Au layer was used as the OBL, the sample showed no RS behavior even though the rectifying behavior was still maintained. This is identical behavior to that of the sample with no OBL ME is composed of one 30-nm-thick Pt layer, of which an *I–V* curve and cross-section SEM image are shown in Figure S2a,b, respectively (Supporting Information). When the oxygen vacancy concentration is too high in the URS memory cell, the whole area of the film becomes too electrically leaky to support a localized current flow that is necessary to induce conducting filament (CF) formation and subsequent rupture. Therefore, adoption of an appropriate OBL is a prerequisite in achieving well-performing stacked SD/URS memory devices. As can be understood in Figure 2a the 30-nm-thick Ni layer works appropriately, so the fluent URS operation with suppressed current in the negative bias voltage region was obtained. Other OBL materials such as $(In,Sn)O_x$ and TiN were also tested, and their switching *I–V* curves are shown in Figures S3a,b, respectively (Supporting Information). Among them, the Ni OBL showed the best electrical performance, and the fabrication process with Ni was easier since simple electron beam evaporation could be used. Therefore, the 30-nm-thick Ni was adopted as the OBL. Due to the suppression of oxygen diffusion from the memory into the SD when OBL was adopted, the reverse current was slightly increased as can be seen in Figure 2a. However, the thickness of the thermal ALD TiO_2 layer in the SD played a more crucial role in determining the rectification ratio. Figure S4 (Supporting Information) shows the switching *I–V* characteristics of the stacked 32 × 1 CA devices with varying thermal ALD TiO_2 thickness in the SD (21, 28, and 31.5 nm). The rectification ratio of the device was improved with increasing TiO_2 thickness (3×10^3 at 1.58 V, 2×10^4 at 1.86 V and $\approx 10^5$ at 1.93 V for 21, 28 and 31.5 nm, respectively), while the forward current was minimally influenced and the increase in the switching voltage was not large too. Even though the rectification ratio of $\approx 10^5$ for the 31.5-nm-thick TiO_2 was not as high as that of only the SD (> approx. 10^6), perhaps due to various process-induced degradations, it was still a viable value to test the performance of the 32 × 32 CA device in this work. In fact, further increase in the TiO_2 thickness in the SD made the selection of appropriate switching voltages difficult during the pulse switching test using the present measurement setup. Therefore, the fabrication of the stacked CA devices proceeded with the 30-nm-thick Ni OBL and 31.5-nm-thick thermal ALD TiO_2 in the SD. Thicknesses of other layers did not influence the device performance largely.

3. Performance of Stacked 1D1R Device Without Parallel Current Paths

Before examining the performance of the CA device with the stacked SD/URS memory cells with large numbers of parallel current paths, the electrical performances of the stacked SD/URS memory cell were studied using a structure of 32 × 1 type 1D1R CA with various line widths (2, 4, 6, 8, and 10 μm). In this configuration, there are no parallel current paths, so the influence of the SD on the URS memory can be examined without interference from the sneak current. **Figure 3**a shows the switching *I–V* curves of the devices with the varying line width, and Figure 3b summarizes the rectification ratio (maximum ratio between the ON-state current in the positive bias region and reverse current in the negative bias region) and RESET current for the different active areas of the devices (= (line width)^2). During the measurements in voltage sweep mode, a compliance current (I_{cc}) of 5 mA was used to protect the samples from complete breakdown. A sufficiently large rectification ratio of $\approx 1 \times 10^5$ was obtained irrespective of the

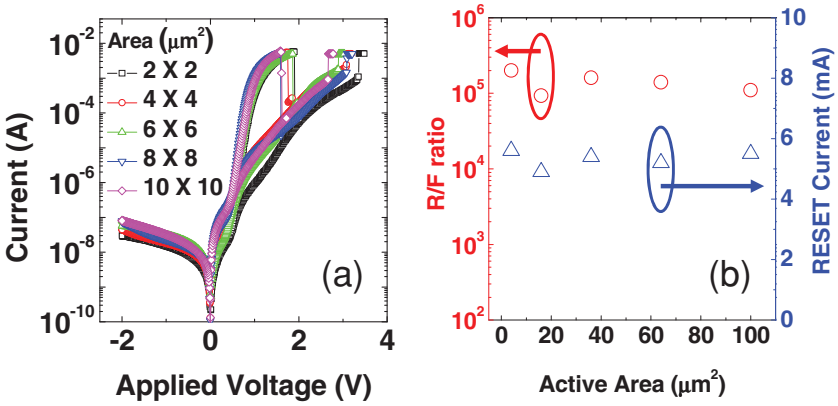

Figure 3. a) The switching DC I-V curves of stacked SD/URS memory cell, studied using a structure of 32 × 1 type 1D1R CA with various line widths (2, 4, 6, 8, and 10 μm). b) The summarized results of the rectification ratio (maximum ratio between the LRS current in positive bias region and reverse current in the negative bias region) and RESET current for the different active areas of the devices (= (line width)^2).

active area of the devices (2×10^5 at 1.86 V, 9×10^4 at 1.85 V, 1.5×10^5 at 1.69 V, 1.3×10^5 at 1.6 V and 1×10^5 at 1.55 V for 4, 16, 36, 64 and 100 μm^2 of active area, respectively). The reverse-state current is independent of the memory state of the URS memory cell, which is indeed the desired performance of the stacked 1D1R CA device. In addition, the RESET current was also independent of the active area of the device, demonstrating that the local current conduction mechanism based on CF formation and rupture as in the much larger-area samples works here. The other notable finding from these switching *I–V* curves is the similarity between the SET current (which is I_{cc}) and RESET current (maximum current level immediately prior to the RESET occurs). For the given I_{cc} of 5 mA, the RESET current remained at 6–7 mA irrespective of the active area. An excessive RESET current level of oxide-based ReRAM compared with the SET current has been one of the most serious obstacles for application. The higher level of RESET current compared with the SET current is a somewhat natural consequence of the switching mechanism; SET is more dependent on the electric field driven behavior of ions, while RESET mostly relies upon thermal energy.[22–28] However, in actual application, the involvement of many parasitic components from the circuit, especially capacitive components, makes the precise control of CF formation during SET difficult, which almost always makes the CF too strong to be ruptured during the subsequent RESET step with just enough power (or RESET current) to rupture the CF if it was formed just enough to maintain the SET state. This problem was actually observed in this work too; the RESET current was much higher (≈11 mA) compared with the SET current as shown in Figure S1c (Supporting Information) when no SD was integrated with the URS memory. This suggests that the integration of the SD actually improved this problem quite considerably. The resistance of SET state of the stacked 1D1R device, which was ≈300–400 Ω (at 1.5 V) as shown in **Figure 4**a, was around ten times larger than the resistance of SET state of only 1R, which is typically ≈10–30 Ω, irrespective of the device area. The forward state resistance of the SD is 250 Ω (at 0.7 V) or 45 Ω (at 1 V). This means that the SET state resistance of the memory in the stacked device is ≈250–350 Ω meaning that the forward state resistance of the SD played a role as a buffer resistor suppressing the excessive current flow during the SET step making the CF just strong enough to sustain the low resistance of the SET state.[28] With the buffer resistor, a large portion of the applied voltage becomes applied to the buffer resistor immediately after the SET switching starts to occur, which prevents the excessive growth of CF. On the other hand, if the CFs are weakly formed, they are prone to the unwanted rupture by thermal or electrical noise during the retention period, making the SET state unstable. However, the high forward resistance of the SD at low voltage region appears to block out these noise components and the retention is very stable as shown in Figure 4b. In fact, the connection of external resistance (R_{ext}) with a constant value to the memory cell to protect the memory from the excessive current flow during SET and noise during the retention has been reported.[29] However, this can also cause problems in RESET as is described well elsewhere;[30] a constantly high R_{ext} prevents stable RESET due to the immediate redistribution of applied voltage after the RESET, or at least it makes the voltage margin for the SET and RESET smaller. However, the forward state resistance of the SD is highly voltage-dependent, as shown in the inset of Figure S1b (Supporting Information). It is higher in the low voltage region, which is beneficial in protecting the memory from the noise components during retention, but is lower in the high voltage region, which minimally interferes with the RESET switching operation. Therefore, the adoption of the SD diode in for the URS memory is actually highly beneficial for the stable operations of the SET and RESET with lower power.

Figure 4a,b show the switching endurance and retention characteristics (line width of 10 μm) measured at room temperature and 80 °C, respectively. While the retention data was satisfactorily stable (almost no time dependence perhaps due to the protection effect of SD), the endurance performance still remained at only 200–300 cycles. Since the endurance failure is intimately related to the loss of oxygen from the memory cell, it was expected that the overlying structure of the SD on top of the URS memory could enhance the endurance. The authors previously reported on a CA-type TiO_2-based RS memory cell without an SD endured ≈150 switching cycles before failure.[31] The failure occurred in both SET- and RESET-stuck modes, which is also the case here. Therefore, the endurance of the stacked device was slightly improved, although the general level is still too low compared with the necessary level for device application. However, it needs to be noted that the promising endurance results reported from other materials always used optimized pulse switching parameters to minimize the damage effect,[32,33] which is not taken in this work.

From the results up to now, it is evident that the integration of SD with the URS memory cell is actually beneficial in improving the device performance in addition to its original intention of suppressing the sneak current. Actual CA performances

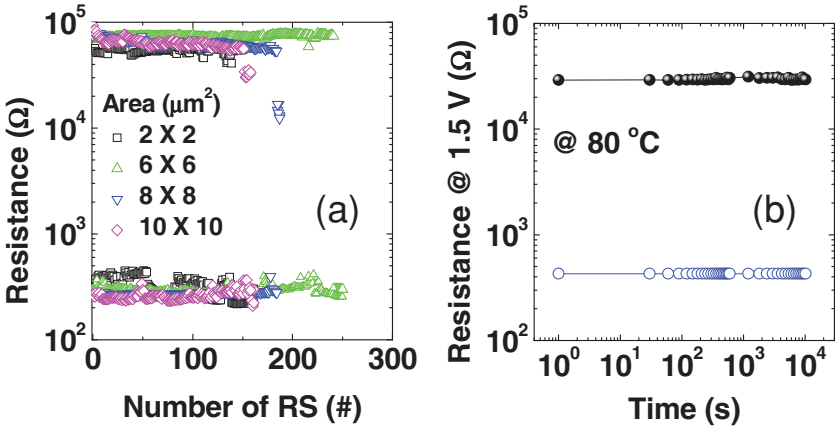

Figure 4. a) Switching endurance and b) retention characteristics (line width of 10 μm) measured at room temperature and 80°C, respectively.

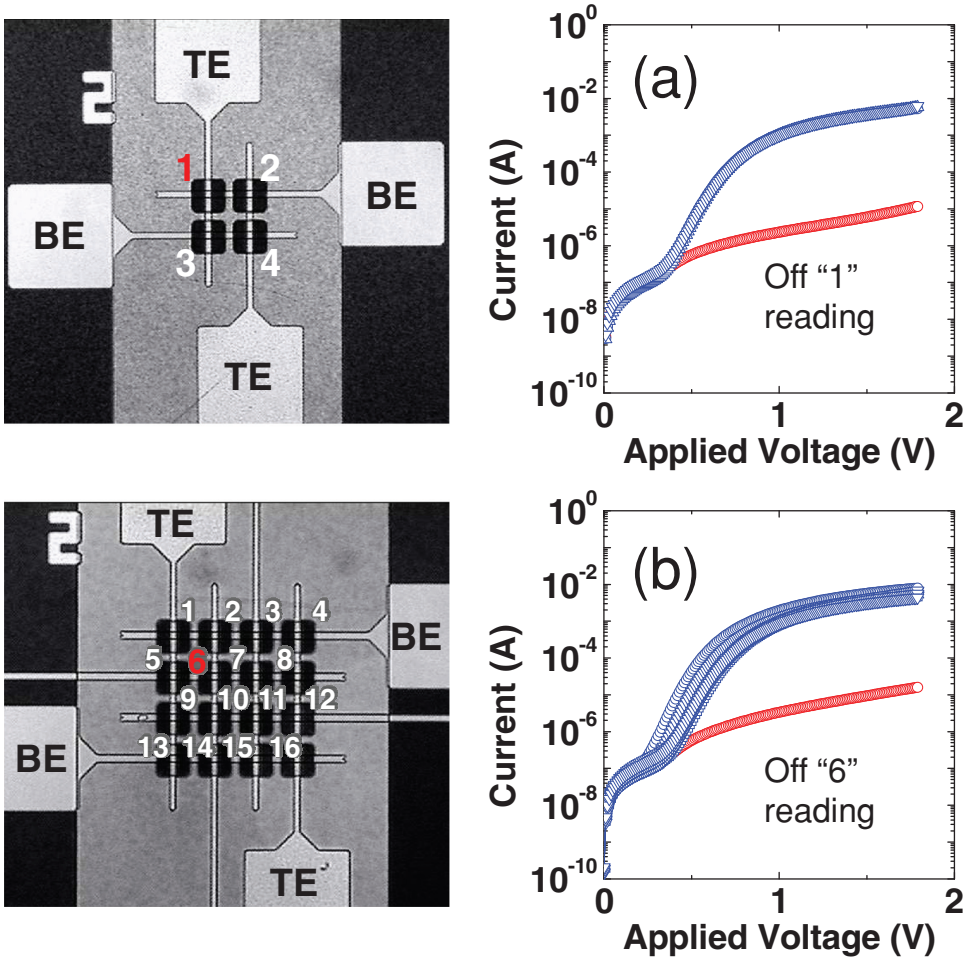

Figure 5. The worst case reading operation of one selected cell in a) 2 × 2 and b) 4 × 4 1D1R CA devices. Left-hand panels show the optical microscopy image of the devices, and right-hand panels show the *I–V* curves of the LRS and HRS cells.

with parallel current paths ($m \times n$ configuration, where m and $n > 1$) are described in next section.

4. Stacked 1D1R CA Device with Parallel Current Paths up to 32 × 32

Before testing the RS performances of the highest density CA device (32 × 32) in this work, the direct current (DC) performances of the lower density CA devices were examined. **Figure 5**a,b show "the worst case" reading operation of one selected cell in 2 × 2 and 4 × 4 1D1R CA devices, respectively. For this test, all the memory cells were switched to LRS first by electroforming. Then, the selected cells (numbers 1 and 6 in each case, left hand optical microscopy image) are switched into HRS by a voltage sweep while all other cells remain in LRS. While all other cells show high current, the target cells show low current in the subsequent *I–V* sweep to examine the resistance state as shown in the right hand panels. This means that all the sneak current paths were efficiently blocked by the integrated SD.

Next, a pulse switching test was performed, the conditions of which are much closer to the actual operation of the memory device. The measurement set up and its equivalent circuit model for the pulse switching test was shown in the inset figure of Figure S6a,b (Supporting Information). Compared with the DC voltage sweep test, such pulse test requires optimization of the pulse height and width to appropriately examine the SET and RESET performances. Therefore, the simplest 2 × 2 type of the 1D1R CA was taken and the necessary SET pulse height and width were examined. Figure S5a,b (Supporting Information) show the variations of the SET and RESET state resistances measured at 1.5 V, and RESET time (the time needed for resistance switching from LRS to HRS) according to SET pulse height and width, respectively. Here, the RESET pulse height was fixed at 3.5 V and the RESET time was estimated by monitoring the current flow through the sample using a digital oscilloscope (OSC) as shown in **Figure 6**a. The SET pulse width and height in Figure S5a,b (Supporting Information) were 500 ns and 4 V, respectively. The appropriate range for RESET pulse height was very limited, to only ≈3.4–3. 6 V. With no SD integrated, the RESET by the pulse application was almost impossible irrespective of

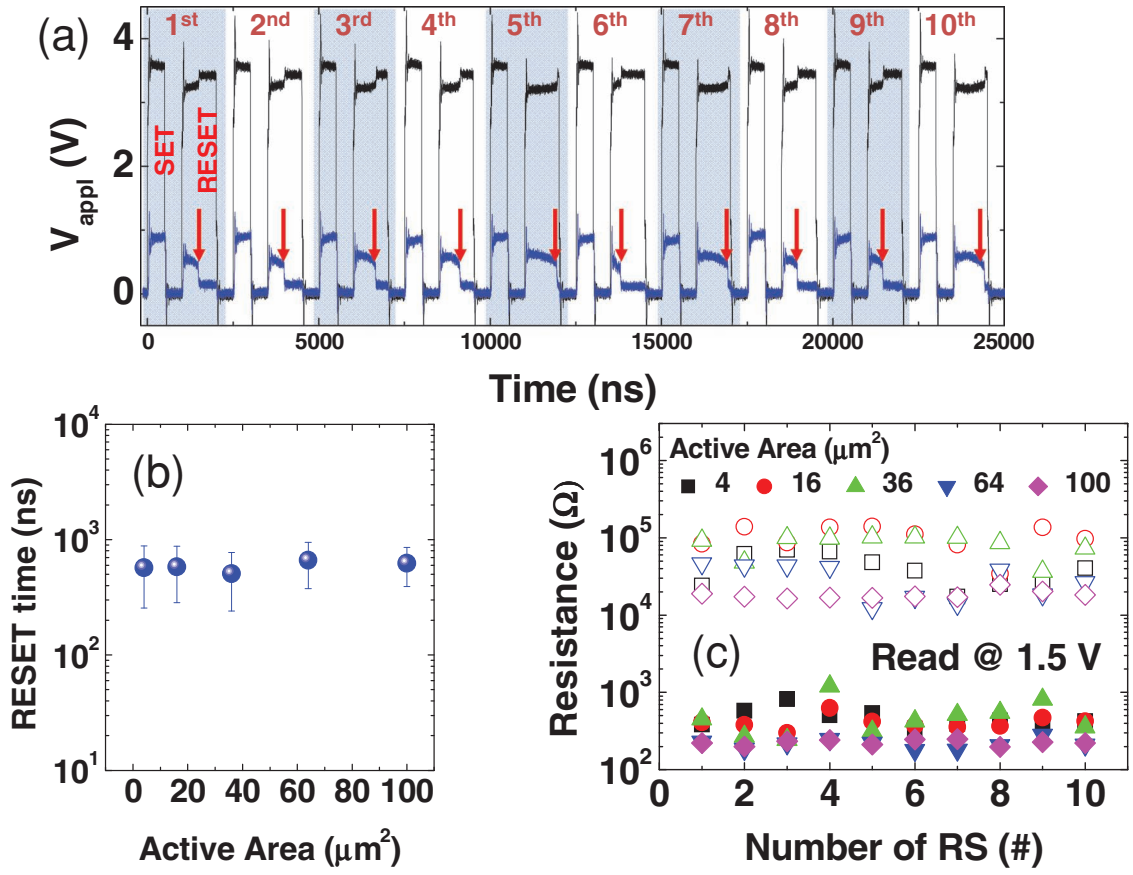

Figure 6. a) The electrical response monitored by OSC when the SET and RESET pulses were applied to 100 μm^2 of active area. b) The variation of RESET time as a function of active area. c) Resistance distribution of LRS and HRS of 1D1R CA with various active areas.

the pulse height and width. This was ascribed to the parallel configuration of the pulse generator (HP 81110A) where there is always a parallel current path connected to ground via the internal resistance of the equipment (50 Ω) in addition to the sample (see Figure S6b, Supporting Information). When the sample starts to RESET, making the sample resistance much higher than the internal resistance, most of the supplied current flows through the parallel current path, and the complete RESET of the sample is inhibited. This is not the case in DC sweep using the semiconductor parameter analyzer (SPA), which does not contain such a parallel current path. If an excessive voltage was programmed to the pulse source, the unstable RESET fluctuation between RESET and SET states occurs due to the presence of internal OSC resistance (50 Ω), which works as a constant serial R_{ext}. It appears that the weakly formed CF in the URS memory of the stacked 1D1R device in this study can be fluently ruptured even with the small current in the pulse switching test, which again manifests the fluent functionality of this 1D1R memory.

As shown in Figure S5 (Supporting Information), the long duration and high amplitude of the electric voltage pulse for SET operation brought about increased RESET time. The RESET time varied from ≈250 ns to ≈1000 ns depending on the SET pulse conditions. While the resistance of the HRS was not influenced much, that of LRS was decreased slightly with increase in pulse height and width, meaning that stronger CFs were formed. When the SET pulse height and width were respectively 4 V and 50 ns, the RESET time was as short as ≈250 ns, but such a short SET pulse was vulnerable to interference by circuit noise, as shown in Figure S6 (Supporting Information). From these results, therefore, the appropriate SET and RESET pulses to examine the device performance were determined to be 4 V/500 ns and 3.5 V/1000 ns, respectively.

Next, the active area dependence of RESET time and resistances of LRS and HRS were tested using the 2 × 2 type 1D1R CA with various areas (4, 16, 36, 64, and 100 μm^2). In each active area, ten consecutive SET and RESET switching cycles were performed using the above mentioned pulses, and the resistances of LRS and HRS were read at 1.5 V by SPA at each RS event. Figure 6a shows the electrical response monitored by OSC when the SET and RESET pulses were applied to 100 μm^2 of active area. The black and blue lines show the transient voltage signal read from channel 1 (Ch1) and channel 2 (Ch2) of the OSC, which represent the input signal from a pulse generator and signal from the sample, respectively (see Supporting Information for more detailed interpretation of this measurement setup.). Because the voltage difference between Ch1 and Ch2 represents the voltage drop across the 1D1R CA device (V_{sample}), the increase or decrease of the difference between two transient pulses corresponds to the RESET

or SET events of 1D1R CA, respectively. The RESET event showed obvious increase in V_{sample} at the moment that RESET occurs, indicated by red arrows so that the RESET time can be easily determined from the OSC signal. On the other hand, the voltage variation while applying the SET pulse was not observed even though the sample certainly showed LRS after the SET pulse application. It is believed that the SET time is very short (<50 ns), which is hardly observed with the present setup. This is consistent with the previous results of Choi et al.,[34] where only a few tens of ns for SET time were observed in a TiO_2-based RS cell. Figure S6a–c (Supporting Information) show the variation of voltages in Ch1 and Ch2 for the SET pulses with different width. Detailed discussions are also included in the Supporting Information. The data in Figure 6b show the variation of RESET time with active area. The average RESET time was ≈500–600 ns, irrespective of the device area, which is longer than the SET time by more than one order of magnitude. As mentioned above, this is because the SET process is driven mostly by the electric field, but the RESET process is accomplished mostly by thermally driven chemical reaction. Meanwhile, the estimated RESET time of ≈500–600 ns is much shorter than that observed in the same TiO_2 URS memory cell without the SD (several μs to 100 μs) reported by Choi et al.[34] Again, this can be ascribed to the weakly formed but still stable CF in the memory cell of the present work. The localized RS characteristic can be confirmed in Figure 6c, where the resistance of LRS is almost independent of the active areas. While the area-independent resistance of LRS is strong evidence for the localized switching mechanism mediated by CF, the electrode area can actually have non-negligible influence on the resistance of LRS via the capacitive charging effect, as has been discussed in detail independently by Song et al.[35] and Kinoshita et al.[29] In short, the RS memory in HRS resembles a capacitor that stores charges during the bias application for the SET switching. At the moment of SET, the stored charge starts to dissipate through the forming CF, which further strengthens the CF, by which the electrode area can influence the resistance of CF. Here, the active area varies by up to a factor of 25 (between 4 and 100 μm^2), so this influence can be substantial. However, in case of 1D1R CA, the stacked SD decreases the total capacitance of the memory cell and the resistance of the forward SD increases the RC-delay time of the device compared to the RS element alone. These effects diminish the capacitive charging effect on the SET switching, which again manifests the positive influence of the SD. The resistance of HRS appears to decrease slightly with the increasing active area, which might be explained by the increased leakage current through the larger area, except for the smallest area case. The smallest one appears to be influenced by the geometry effect.

Figure 7 shows the RS properties of one selected cell with various resistance states of neighboring unselected cells in the 2 × 2 1D1R CA device. It is important to examine the RS characteristics of a target memory cell in terms of not only the resistance ratio but also the RS operation time according to the various memory states of unselected cells. For this test, the target memory cell was numbered as 4 while the others were numbered 1, 2, and 3 among the 2 × 2 cells (Figure 7a). In this case, there could be eight different configurations as shown in Figure 7d. For each configuration, the RS of the selected unit cell was performed three times as shown in Figure 7b,c for the cases where all other cells were in HRS and LRS, respectively, and the results are summarized in Figure 7d. It was confirmed that the resistance ratio and RESET time are independent from any combined resistance states of the unselected cells.

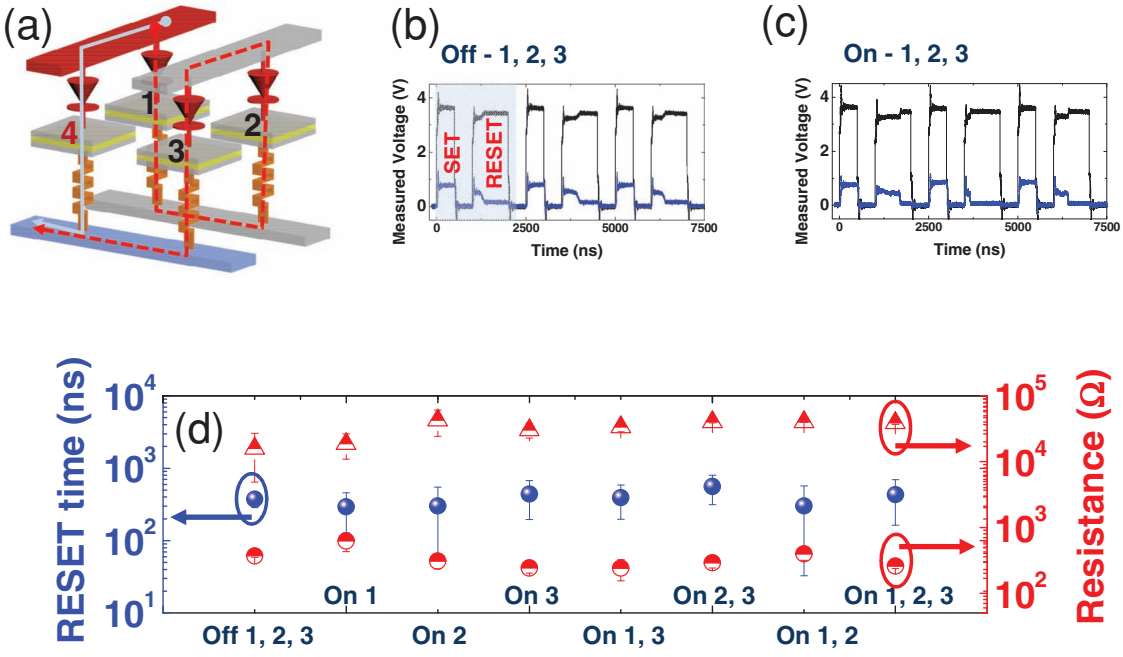

Figure 7. a) Schematic diagram of 2 × 2 type of 1D1R CA device. b,c) Transient pulses monitored by OSC when all the unselected cells are in the off and on state, respectively. d) Summary of resistances of LRS/HRS and RESET time with various resistance states of unselected cells.

This demonstrates that the stacked SD very effectively suppresses the parasitic effect from the neighboring unselected cells in the 1D1R CA device. The possible parasitic effects in the 1D1R CA device are sneak current through the low resistance leakage paths along the unselected cells, and parasitic capacitance effect from the unselected cells in parallel connection with the selected cell. While the reading operation can be disturbed by the former, parasitic capacitance can affect the writing operation.[29,35] The parasitic capacitance effects of the worst case in the 2 × 2 type 1D1R CA device can be considered as that the unselected cells being serially connected to the target cell when all the other interconnection lines, except for selected interconnection lines, are electrically floated (see Figure 7a). Three unselected cells are composed of three LRS memory element, two forward SDs, and one reverse SD. Then, the capacitive component of these parasitic elements is dominated by the capacitance of reverse SD because the LRS memory and forward SD are mostly resistors. Due to the fully depleted configuration of the SD under the reverse bias condition, the overall capacitive component of the 1D1R memory cell can be largely diminished. Consequently, the selected cell in the 2 × 2 type of 1D1R CA can show stable RS performance regardless of the resistance state of the unselected neighboring cells.

The parasitic effects from the CA are further examined using a CA device with a much higher density (32 × 32). There could be two kinds of possible parasitic capacitances in 1D1R CA. One is the capacitance coupling effect between neighbored interconnection lines, and the other is the capacitive charges from unselected cells. Considering that the distances between the interconnection lines are of several micro-meters and the thickness of the lines is only ≈100 nm, the capacitive coupling effect between parallel interconnection lines can be ignored. Therefore, study on the parasitic capacitance effect is focused with this larger scale device, although its negligible influence has already been demonstrated in Figure 7 with smaller array density. The test structure is the 32 × 32 type of 1D1R CA device with 10-μm line width (SEM image of the device is shown in **Figure 8**d), and the RS characteristic of one selected cell was examined with the increasing number of LRS cells near the target cell up to 20 × 20 (testing all the 32 × 32 cells takes too long to do). As shown in Figure 8a, the resistance ratio and RESET time of the selected cell are almost invariant regardless of the number of unselected LRS cells. This result shows that the stacked SD enhances the ability to suppress the parasitic effect from unselected cells not only for the reading but also for the writing operation. The *I*–*V* curves shown in Figure 8b,c show the electrical characteristic of the selected cell

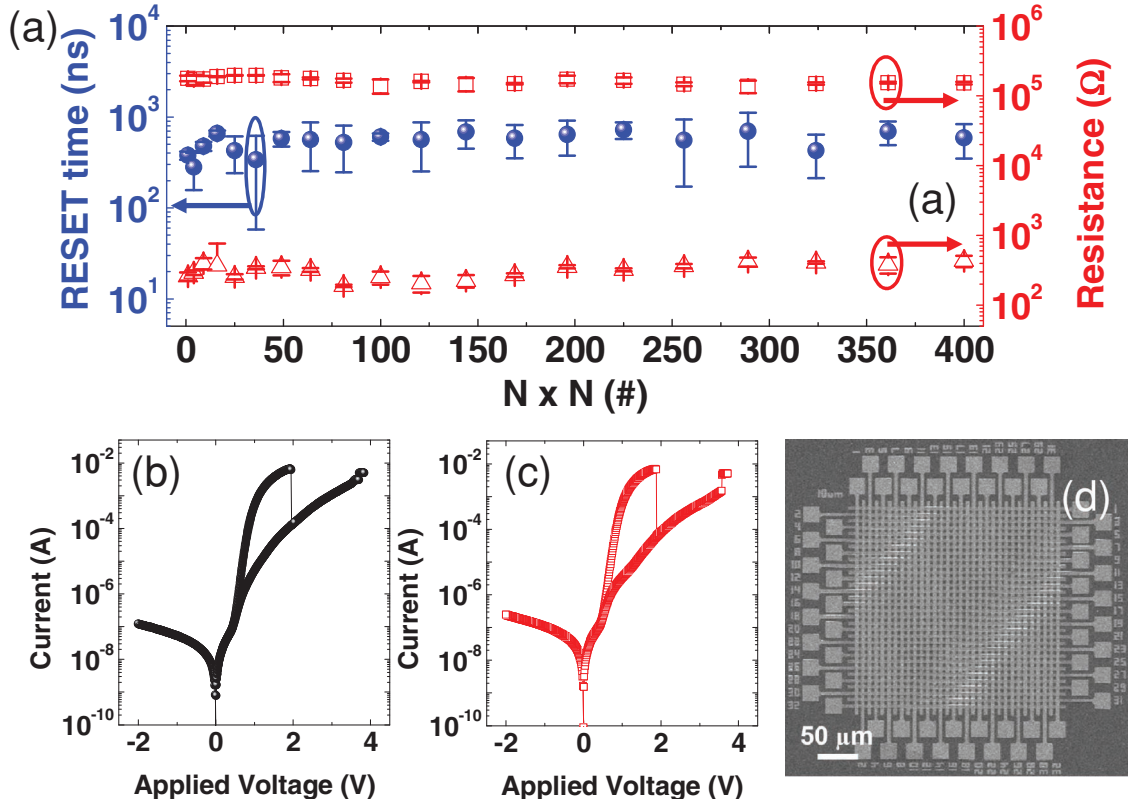

Figure 8. Summary of resistances of LRS/HRS and RESET time as a function of the number of unselected cells which are in LRS. b,c) Electrical characteristics of the selected cell obtained by SPA when all the neighboring 20 × 20 unselected cells are switched to LRS and HRS, respectively. d) SEM image of 32 × 32 1D1R CA device with 10-μm line width.

obtained by SPA when all the neighboring 20 × 20 unselected cells are switched to LRS or HRS, respectively. It was confirmed that there were no variations in the *I–V* characteristics of the selected cell irrespective of the resistance states of the many neighboring cells. This shows the promise of the role of SDs in 1D1R CA devices.

5. Conclusion

In conclusion, 1D1R CA devices composed of stacked SD (Pt/TiO_2/Ti/Pt) and URS memory (Pt/TiO_2/Pt) elements were fabricated, and their fluent functionality as ReRAM was proved. For the fabrication of the stacked devices, the adoption of an appropriate oxygen barrier layer, which in this case was 30-nm-thick Ni, was of prime importance to retain desirable performance of the SD (high rectification ratio of $\approx 10^5$) and URS memory (resistance ratio $\approx 10^3$). From the electrical characterization of the single stacked device structure, which is fundamentally free from the interference effect, the adoption of the SD was proven to be quite beneficial in achieving fluent RS properties of the memory element in addition to the intended purpose of the SD of suppressing the sneak current. It was found that the appropriate forward resistance of the SD during the SET switching allowed the formation of sufficiently weak CF, which in turn allowed fluent RESET switching with low energy. The sufficiently low forward resistance of the SD at the RESET voltage also did not interfere with the RESET operation. On the other hand, the much higher resistance of the SD during the retention period protects the weak CF from thermal or electrical noise, making the retention excellent. The appropriate pulse conditions for the pulse switching were determined from the 2 × 2 and 4 × 4 CA devices, and these conditions were used to test the 32 × 32 1D1R CA devices. The adopted SD sufficiently blocks the adverse interferences from all the unselected neighboring cells, which allows the pulse switching characteristics to essentially be independent of the array size (density) and active area. With the SET and RESET pulse voltages of 4 and 3.5 V, SET time less than 50 ns and RESET time of 500–600 ns were achieved. The random access of each cell was also confirmed. This work reveals that the 1D1R CA device with SD and URS memory can be a promising structure for ReRAM, though further improvement in endurance is necessary.

6. Experimental Section

Various 1D1R CA array types (32 × 1, 2 × 2, 4 × 4, and 32 × 32) with line widths of 2, 4, 6, 8 and 10 μm were fabricated as an experimental demonstration. The top and bottom electrode (TE and BE, respectively) have stacks of Au(50 nm)/Pt(50 nm) and Pt(50 nm)/Au(50 nm), respectively. The Au layers of each TE and BE were added for reducing the interconnection line resistance in CA.[30] As shown in Figure 1b, the 14 × 14 μm^2 of the middle electrodes (ME), which were electrically isolated from each other, was fabricated with stacks of Pt(30 nm)/Ni(30 nm)/Pt(30 nm) between every SD and RS cell in the 1D1R CA. The Ni layer was utilized as an oxygen barrier layer. The 100-nm-thick Ti layer of the SD used as an active layer was electron-beam evaporated with growth rate of 1 nm/s at $\approx 10^{-7}$ Torr immediately after the ME deposition to achieve the self-aligned structure by the subsequent lift-off process. All the electrodes of the 1D1R CA were patterned by conventional photo-lithography followed by electron beam evaporation and lift-off processes. The TiO_2 thin films for the RS (60 nm) and active layer of the SD (31.5 nm) were deposited by plasma-enhanced and thermal atomic layer deposition (ALD) using $Ti(OC_3H_7)_4$ precursor with plasma-activated O_2 and O_3 as the oxygen source, at a wafer temperature of 250 °C, respectively. The ALD with plasma-activated O_2 provided the TiO_2 films having more fluent RS performance, while the ALD with O_3 provided the TiO_2 films having higher diode performance. The film thickness was measured by an ellipsometer (Gaertner Scientific Corporation) using the TiO_2 films deposited simultaneously on Pt substrate. The details of each of the ALD processes of TiO_2 are reported elsewhere.[36,37] Stable electrical BE contact was achieved by etching the TiO_2 layer over the contact area using a reactive ion etching process.

The resistive switching behavior of the 1D1R CA device was measured using a HP4145B semiconductor parameter analyzer at room temperature in voltage sweep mode. Each voltage sweep began from 0 V and the bias was applied to the TE while the BE was grounded. During the SET switching experiment, 5 mA of current compliance was applied to protect the cells from complete breakdown. The RS endurance characteristics were also examined by voltage sweep mode at room temperature. The retention characteristic was investigated up to 10^4 seconds at 80°C with reading voltage of 1.5 V. For RS speed measurement, the transient voltage was monitored using a digital oscilloscope (OSC, Tektronix 684C) while an electric pulse was applied by a pulse generator (HP81110A). The cross-sectional and surface topologies of the fabricated 1D1R CA device were monitored by a scanning electron microscope (SEM, S-4800, Hitachi) and scanning probe microscope (SPM, JSPM-5200, JEOL), respectively.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This study was supported by the National Research Program for Nano Semiconductor Apparatus Development sponsored by the Korea Ministry of Knowledge and Economy (10034831), and the Global Research Laboratory program (2012040157) through the National Research Foundation (NRF) of Korea.

Received: August 1, 2012
Revised: August 30, 2012
Published online: October 18, 2012

[1] R. Waser, M. Aono, *Nat. Mater.* **2007**, *6*, 833.
[2] D. B. Strukov, G. S. Snider, D. R. Stewart, R. S. Williams, *Nature* **2008**, *453*, 80.
[3] R. Waser, R. Dittmann, G. Staikov, K. Szot, *Adv. Mater.* **2009**, *21*, 2632.
[4] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, R. S. Williams, *Nature* **2010**, *464*, 873.
[5] A. Sawa, *Mater. Today* **2008**, *11*, 28.
[6] E. Linn, R. Rosezin, C. Kugeler, R. Waser, *Nat. Mater.* **2010**, *9*, 403.
[7] M. J. Lee, S. Seo, D. C. Kim, S. E. Ahn, D. H. Seo, I. K. Yoo, I. G. Baek, D. S. Kim, I. S. Byun, S. H. Kim, I. R. Hwang, J. S. Kim, S. H. Jeon, B. H. Park, *Adv. Mater.* **2007**, *19*, 73.
[8] E. Ping, Y. Erokhin, H. Gassmann, F. A. Khaja, *Junction Technol. (IWJT), 2012 12th Int. Workshop* **2012**, 24.
[9] J. I. Lee, H. Park, S. L. Cho, Y. L. Park, B. J. Bae, J. H. Park, J. S. Park, H. G. An, J. S. Bae, D. H. Ahn, Y. T. Kim, H. Horii, S. A. Song, J. C. Shin, S. O. Park, H. S. Kim, U-In Chung, J. T. Moon, B. I. Ryu, *VLSI Technol. Symp.* **2007**, 102.

[10] W. Y. Park, G. H. Kim, J. Y. Seok, K. M. Kim, S. J. Song, M. H. Lee, C. S. Hwang, *Nanotechnology* **2010**, *21*, 195201.
[11] Y. C. Shin, J. W. Song, K. M. Kim, B. J. Choi, S. Choi, H. J. Lee, G. H. Kim, T. Y. Eom, C. S. Hwang, *Appl. Phys. Lett.* **2008**, *92*, 162904.
[12] N. Huby, G. Tallarida, M. Kutrzeba, S. Ferrari, E. Guziewicz, Ł. Wachnicki, M. Godlewski, *Microelectron. Eng.* **2008**, *85*, 2442.
[13] G. H. Kim, J. H. Lee, J. H. Han, S. S. Song, J. Y. Seok, J. H. Yoon, K. J. Yoon, M. H. Lee, T. J. Park, C. S. Hwang, *Appl. Phys. Lett.* **2012**, *100*, 213508.
[14] J. H. Lee, G. H. Kim, Y. B. Ahn, J. W. Park, S. W. Ryu, C. S. Hwang, H. J. Kim, *Appl. Phys. Lett.* **2012**, *100*, 123505.
[15] S. H. Chang, S. B. Lee, D. Y. Jeon, S. J. Park, G. T. Kim, S. M. Yang, S. C. Chae, H. K. Yoo, B. S. Kang, M. J. Lee, T. W. Noh, *Adv. Mater.* **2011**, *23*, 4063.
[16] M. D. Pickett, R. S. Williams, *Nanotechnology* **2012**, *23*, 215202
[17] J. J. Yang, M.-X. Zhang, M. D. Pickett, F. Miao, J. P. Strachan, W.-D. Li, W. Yi, D. A. A. Ohlberg, B. J. Choi, W. Wu, J. H. Nickel, G. Medeiros-Ribeiro, R. S. Williams, *Appl. Phys. Lett.* **2012**, *100*, 113501.
[18] A. N. Morozovska, E. A. Eliseev, S. L. Bravina, F. Ciucci, G. S. Svechnikov, L.-Q. Chen, S. V. Kalinin, *J. Appl. Phys.* **2012**, *111*, 014107.
[19] G. H. Kim, K. M. Kim, J. Y. Seok, H. J. Lee, D. Y. Cho, J. H. Han, C. S. Hwang, *Nanotechnology* **2010**, *21*, 385202.
[20] A. Flocke, T. G. Noll, *Proc. 33rd Eur. Solid-State Circuits Conf.*, **2007**, 328.
[21] K.-H. Kim, S. Gaba, D. Wheeler, J. M. Cruz-Albrecht, T. Hussain, N. Srinivasa, W. Lu, *Nano Lett.* **2012**, *12*, 389.
[22] D. Matthew, J. Borghetti, J. J. Yang, M. Gilberto, R. S. Williams, *Adv. Mater.* **2011**, *23*, 1730.
[23] S. H. Chang, S. B. Lee, D. Y. Jeon, S. J. Park, G. T. Kim, S. M. Yang, S. C. Chae, H. K. Yoo, B. S. Kang, M. J. Lee, T. W. Noh, *Adv. Mater.* **2011**, *23*, 4063.
[24] F. Miao, J. P. Strachan, J. J. Yang, M. X. Zhang, I. Goldfarb, A. C. Torrezan, P. Eschbach, R. D. Kelley, M. Gilberto, R. S. Williams, *Adv. Mater.* **2011**, *23*, 5633.
[25] J. J. Yang, J. P. Strachan, Q. Xia, D. A. A. Ohlberg, P. J. Kuekes, R. D. Kelley, W. F. Stickle, D. R. Stewart, G. Medeiros-Ribeiro, R. S. Williams, *Adv. Mater.* **2010**, *22*, 4034.
[26] M. J. Lee, S. I. Kim, C. B. Lee, H. Yin, S.-E. Ahn, B. S. Kang, K. H. Kim, J. C. Park, C. J. Kim, I. Song, S. W. Kim, G. Stefanovich, J. H. Lee, S. J. Chung, Y. H. Kim, Y. S. Park, *Adv. Funct. Mater.* **2009**, *19*, 1587.
[27] J. J. Yang, I. H. Inoue, T. Mikolajick, C. S. Hwang, *MRS Bull.* **2012**, *37*, 131.
[28] K. M. Kim, D. S. Jeong, C. S. Hwang, *Nanotechnology* **2011**, *22*, 254002.
[29] K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki, Y. Sugiyama, *Appl. Phys. Lett.* **2008**, *93*, 033506.
[30] G. H. Kim, K. M. Kim, J. Y. Seok, M. H. Lee, S. J. Song, C. S. Hwang, *J. Electrochem. Soc.* **2010**, *157*, G211.
[31] G. H. Kim, K. M. Kim, J. Y. Seok, M. H. Lee, S. J. Song, J. H. Yoon, K. J. Yoon, M. H. Lee, K. M. Kim, H. Y. Lee, S. W. Ryu, T. J. Park, C. S. Hwang, *Appl. Phys. Lett.* **2011**, *98*, 262901.
[32] M.-J. Lee, C. B. Lee, D. S. Lee, S. R. Lee, M. Chang, J. H. Hur, Y.-B. Kim, C.-J. Kim, D. H. Seo, S. A. Seo, U. I. Chung, I. K. Yoo, K. N. Kim, *Nat. Mater.* **2011**, *10*, 625.
[33] J. J. Yang, M. X. Zhang, J. P. Strachan, F. Miao, M. D. Pickett, R. D. Kelley, G. Medeiros-Ribeiro, R. S Williams, *Appl. Phys. Lett.* **2010**, *97*, 232102.
[34] B. J. Choi, S. Choi, K. M. Kim, Y. C. Shin, C. S. Hwang, S. Y. Hwang, S. Cho, S. Park, S. Hong, *Appl. Phys. Lett.* **2006**, *89*, 012906.
[35] S. J. Song, K. M. Kim, G. H. Kim, M. H. Lee, J. Y. Seok, R. Jung, C. S. Hwang, *Appl. Phys. Lett.* **2010**, *96*, 112904.
[36] G. J. Choi, S. K. Kim, S. J. Won, H. J. Kim, C. S. Hwang, *J. Electrochem. Soc.* **2009**, *156*, G138.
[37] S. K. Kim, K. M. Kim, D. S. Jeong, W. Jeon, K. J. Yoon, C. S. Hwang, *J. Mater. Res.* DOI: 10.1557/jmr.2012.231.